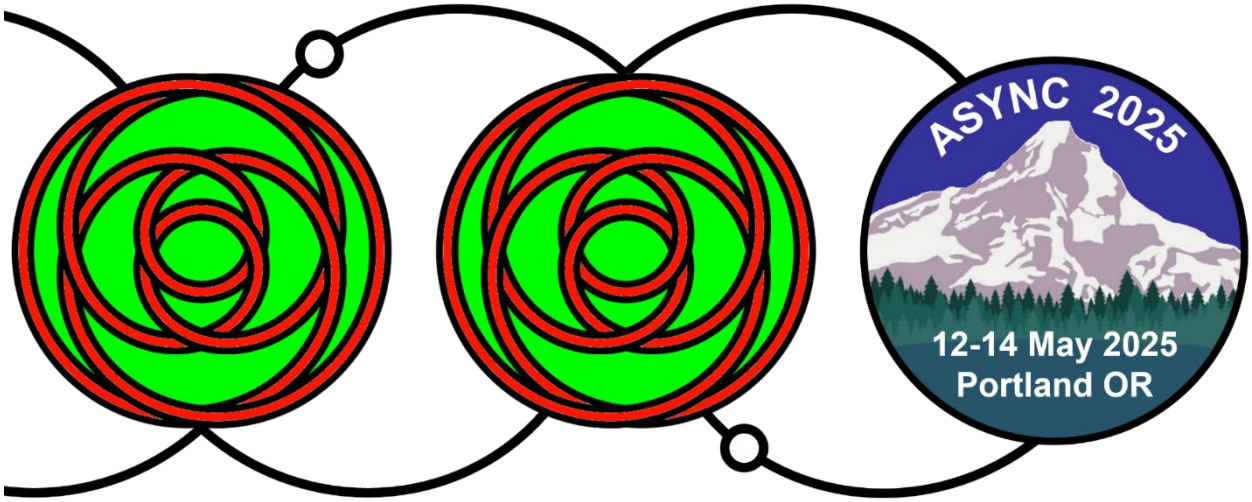
29th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC 2025)



Sunday, 11 May 2025

17:00-18:00: Registration
Lobby of "the Duniway"
The Duniway Portland, a Hilton Hotel
545 SW Taylor, Portland, Oregon, 97204, USA
Phone: +1 (503) 553-7000
Note: *Our original Sunday entry reception has become an exit reception on Wednesday.*

Monday, 12 May 2025

8:30-9:00 Welcome (and registration)

9:00-10:00 Keynote
Chair: Marly Roncken
Keynote 1: Physical Computation in the Era of Hardware Specialization
Jennifer Volk and George Tzimpragos (University of Wisconsin-Madison)

10:00-10:30 BREAK

10:30-12:00 Session 1: Designs I – ASIC
Chair: Ole Richter
10:30-11:00 (#76 – regular)
An Asynchronous RISC-V-based SNN Processor
with Custom ISA Extensions for Programmable On-Chip Learning
Xuanyu Zhang, Jilin Zhang, Haoyang Huang, and Hong Chen

11:00-11:20 (#92 – short Fresh Idea)
Towards the Design of a Radiation-Hardened SNN Accelerator Using SystemVerilogCSP and Chisel
Yuou Qiu, Prahalad Chari, Moises Herrera, Godha Garudaiahgari, Michael Etter, Cole Sherrill, Georgios D. Dimou, and Peter A. Beerel

11:20-11:40 (#109 – short Industry)
Scaledmatx One – A Bundled-Data GALS Inference ASIC
Jon Dama

11:40-12:00 (#110 – short Industry)
Mount Sisyphus: Energy-Efficient Asynchronous RISC-V Microcontroller in Intel 3 Process
Andrew Lines and Ruokun Liu

Monday, 12 May 2025 – CONTINUED

12:00-14:00 LUNCH

14:00-15:00 Session 2: Designs II – FPGA
Chair: Rajit Manohar

14:00-14:30 (#97 – regular)
Efficient FPGA Implementation of Time-Domain Popcount for Low-Complexity Machine Learning
Shengyu Duan, Marcos L. L. Sartori, Rishad Shafik, Alex Yakovlev, and Emre Ozer

14:30-15:00 (#99 – regular) BEST PAPER NOMINEE
A Synthesis Toolflow for the Predictable Implementation
of High-Performance Bundled-Data Asynchronous NoCs on FPGA
Giuseppe Chessa, Elena Bellodi, Michele Favalli, Davide Zoni, and Davide Bertozzi

15:00-15:10 SHORT BREAK

15:10-15:40 Session 3: Mixed Synchronous-Asynchronous Design Aspects
Chair: Ian Jones

15:10-15:40 (#72 – regular)
Distributed Locally Synchronous Grid Oscillator via Perpetual Token Exchange
Josef Salzmann

15:40-16:10 (#95 – regular)
Clock Generator with Clock Domain Crossing
Robert Karmazin, Andrew Lines, Prasad Joshi, and Benjamin Hill

16:10-16:40 BREAK

16:40-17:50 Session 4: New Technologies
Chair: Ken Stevens

16:40-17:10 (#105 – regular)
Muller C-Element for NEMS
Philipp Lehninger, Axel Jantsch, Andreas Steininger, Elliott Worsey, Victor Marot, and Dinesh Pamunuwa

17:10-17:30 (#108 – short Fresh Idea)
Design of an Asynchronous Polymorphic Cryptographic Circuit in 12nm FinFET
Richard Becker, Zhihan Weng, Kelby Haulmark, Nicholas Brown, Kyle Orman, and Jia Di

17:30-17:50 (#111 – short Fresh Idea)
Communication and Guarded Command Modeling of Gate-Level Superconducting Pulse Logic
Marly Roncken

17:50 Closing remarks for Monday
Team up for dinner – check with Local Chairs, Prasad Joshi and Andrew Lines / Steering Committee meeting
… but only after we have taken a GROUP PHOTO.

Tuesday, 13 May 2025

8:30-9:30 Keynote
Chair: Matthias Függer
Keynote 2: Programming Biological Systems across Scales using Synthetic Biology
Thomas E. Gorochowski (School of Biological Sciences, University of Bristol, UK)

9:30-10:00 BREAK

10:00-11:40 Session 5: High- to Low-level Design Tools I
Chair: Georgios Dimou
10:00-10:20 (#74 – short Industry)
Easy async for busy engineers: AFSM-based design of low-latency robust controllers in WORKCRAFT
Danil Sokolov, Victor Khomenko, and Marco Sautto

10:20-10:50 (#94 – regular)
Synthesis and Timing Constraints for Reliable MTNCL Asynchronous Circuits
Cole Sherrill, Ethan Brugger, and Jia Di

10:50-11:10 (#107 – short Fresh Idea/Demo)
Loom: Toward Formal Synthesis of QDI Circuits
Ned Bingham

11:10-11:40 (#102 – regular)
Innovations in MTNCL Gate Design: An Alternative MTCMOS Power-Gating Approach
Cole Sherrill, Kile Harvey, Zhihan Weng, and Jia Di

11:40-12:00 Announcement ASYNC 2026

12:00-14:00 LUNCH

14:00-15:30 Session 6: High- to Low-level Design Tools II
Chair: Mika Nyström
14:00-14:30 (#77 – regular)
Translating General Slack Elastic Programs into Dataflow Circuits
Xiayuan Wen, Rui Li, and Rajit Manohar

14:30-15:00 (#101 – regular)
Asynchronous Design of a Bitwise Elimination Argmax via High-Level Modeling in GRAPHRACK
Hugh Squires-Parkin, Alex Chan, Rishad Shafik, Adrian Wheeldon, and Alex Yakovlev

15:00-15:30 (#75 – regular)
Automated Decomposition of Concurrent Programs for Asynchronous Logic Synthesis
Karthi Srinivasan *and Rajit Manohar*

15:30-16:00 BREAK

16:00-17:00 Session 7: Designs III – Sensors
Chair: Montek Singh
16:00-16:30 (#93 – regular)
Hierarchical Event Readout with Asynchronous Pipelined Opportunistic Merges
Leo Liu and Kwabena Boahen

16:30-17:00 (#100 – regular)
Asynchronous, event-driven readout for large-scale imaging devices
Prafull Purohit and Rajit Manohar

17:00 Closing remarks for Tuesday

18:00-21:00 Dinner Cruise on the Willamette River
Leave Duniway hotel by 18:00 to be safe. Boarding starts at 18:15. The boat departs at 18:30.
If walking is difficult, then please check in advance with Marly Roncken to arrange transportation.

Wednesday, 14 May 2025

8:30-9:30 Honorary Keynote
Chairs: Ivan Sutherland and Alex Yakovlev
Keynote 3: Asynchronous History and Stories
Jens Sparsø (Professor Emeritus, Technical University of Denmark)
Tomohiro Yoneda (Professor Emeritus, National Institute of Informatics in Tokyo)

9:30-10:00 BREAK

10:00-11:50 Session 8: Dedicated Tools: Timing, Layout, Test
Chair: Ben Hill
10:00-10:30 (#85 – regular) BEST PAPER NOMINEE
Post-Placement Timing Optimisations on Asynchronous Designs
Dimitrios Tsalapatas, Nikolaos Chatzivangelis, Christos P. Sotiriou, and Nikolaos Sketopoulos

10:30-11:00 (#96 – regular)
Timing Closure in Relative Timed Asynchronous Designs using Deep Reinforcement Learning
Sumanth Kolluru and Kenneth S. Stevens

11:00-11:20 (#88 – short Fresh Idea/Demo)
Fast and Easy Open-Source Stick Diagram Validation with Stixu
Nicholas Overacker, James Stine, Michal Ptaszynski, Shingo Yoshizawa, and Miho Kobayashi

11:20-11:50 (#87 – regular) BEST PAPER NOMINEE
Investigating the Effects of Permanent Faults in QDI Circuits: A Formal Perspective
Raghda El Shehaby, Matthias Függer, Florian Huemer, Andreas Steininger

11:50-12:00 Submit voting ballot with your Best Paper choice

12:00-14:00 LUNCH

14:00-14:30 Best Paper Award
Chair: Montek Singh – for Best Paper Award Committee: Milos Krstic (Chair), Montek Singh, Laurent Fesquet

14:30-15:00 BREAK

15:00-17:00 Portland Walk (various options)

17:30-20:00 Session 9: ASYNC Community session – CAD, outreach, collaboration, workforce development…
Chair: Prafull Purohit
Light food available from 17:30 to 19:00
Drinks (and BAR) available from 17:30 to 20:00
Those who like to give a DEMO can do so from 17:30 to 18:00
ASYNC Community session starts at 18:00
ASYNC 2025 Closure by 20:00

We thank you for participating and wish you a safe trip back home!

Georgios Dimou and Masashi Imai
ASYNC 2025 General Co-Chairs

Marly Roncken and Matthias Függer
ASYNC 2025 Program Co-Chairs

Prasad Joshi and Andrew Lines
ASYNC 2025 Local Arrangement Co-Chairs

Prafull Purohit
ASYNC 2025 Publicity Chair