



29th IEEE International Symposium on Asynchronous Circuits and Systems

Paper Deadlines

Regular papers:	20 January 2025	(abstract registration)
	3 February 2025	(paper submission)
	10 March 2025	(notification of acceptance)
	31 March 2025	(final version)
Short papers:	24 March 2025	(submission)
	31 March 2025	(notification of acceptance)
	7 April 2025	(final version)

See website for details: <https://asynctsymposium.org/async2025/>

Call for Papers

The International Symposium on Asynchronous Circuits and Systems (ASYNC) is the premier forum for researchers and industry to present their latest insights and results in asynchronous VLSI computing. Asynchronous VLSI computations are at the heart of deep learning, neuromorphic designs, and biological circuits within and between cells. They are particularly well-suited for distributed tasks in fast and low-energy processing and communication and for tasks that require robustness to environmental variations and noise.

We invite you to submit a **6-8 page regular paper** with original scientific work relevant to ASYNC, in IEEE conference format (double-column, 10pt or larger). Author information must be omitted from reviewers. Accepted papers must be presented and will be published in the Symposium Proceedings and the IEEE Xplore Digital Library.

We also encourage you to submit **1-2 page papers for demo-poster-ideas** with a demo or poster abstract or with "fresh ideas" to try out live. These go through a light-weight review. Accepted papers must be presented and will be distributed as handouts at the Symposium.

We solicit **1-4 page papers from industry** on state-of-the-art integration of asynchronous designs to existing or emerging technologies. These must follow the format of a regular paper, but will go through a separate light-weight review process. Accepted papers must be presented and will be published in the Symposium Proceedings and the IEEE Xplore Digital Library.

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